Z0109MA

Logic level four-quadrant triac

Rev. 03 — 4 August 2009 Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate 4-Q triac in a SOT54 plastic package

1.2 Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage of 600V
- Sensitive gate in four quadrants

1.3 Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

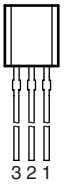
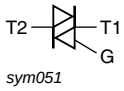
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 38$ °C; see Figure 4 and 1	-	-	1	A
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; T_j = 25 °C; T2+ G-; see Figure 6	-	-	10	mA
		V_D = 12 V; T_j = 25 °C; T2- G-	-	-	10	mA
		V_D = 12 V; T_j = 25 °C; T2+ G+	-	-	10	mA
		V_D = 12 V; T_j = 25 °C; T2- G+	-	-	10	mA

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 SOT54 (TO-92)	 sym051
2	G	gate		
3	T1	main terminal 1		

3. Ordering information

Table 3. Ordering information

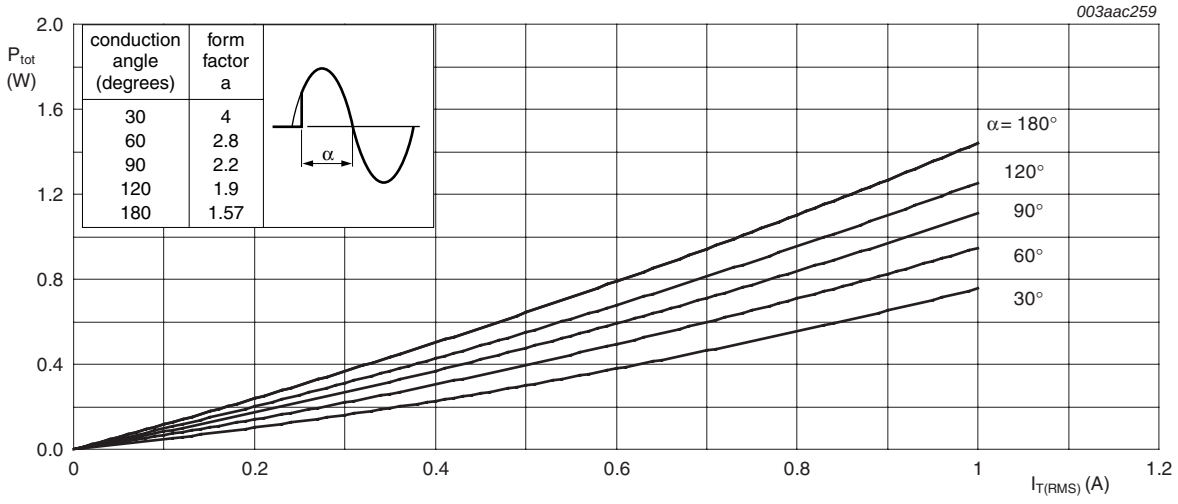
Type number	Package		
	Name	Description	Version
Z0109MA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 4. Limiting values

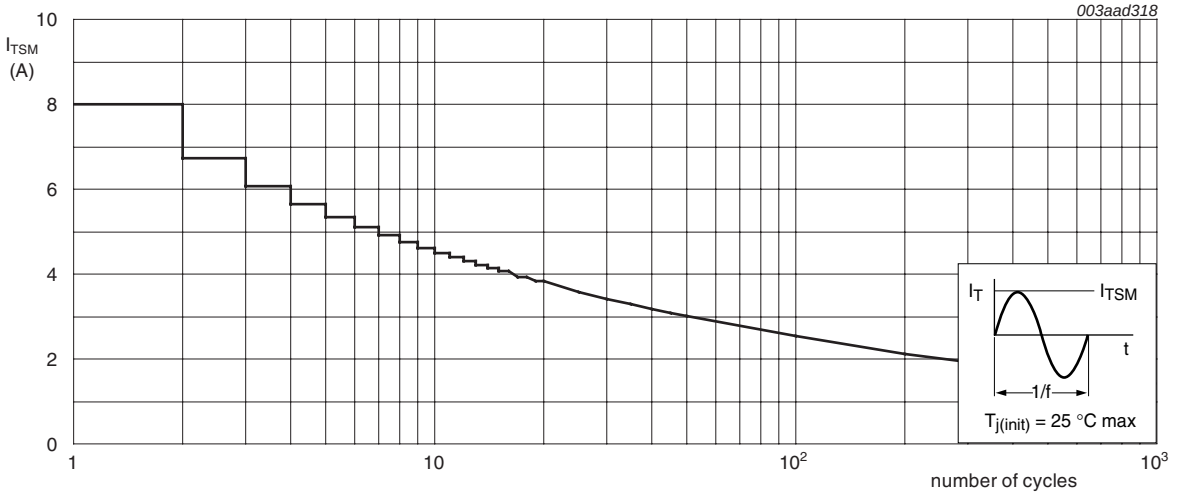
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 38$ °C; see Figure 4 and 1	-	1	A
dI_T/dt	rate of rise of on-state current	I_T = 1 A; I_G = 20 mA; dI_G/dt = 100 mA/µs; T2+ G+	-	50	A/µs
		I_T = 1 A; I_G = 20 mA; dI_G/dt = 100 mA/µs; T2- G+	-	20	A/µs
		I_T = 1 A; I_G = 20 mA; dI_G/dt = 100 mA/µs; T2+ G-	-	50	A/µs
		I_T = 1 A; I_G = 20 mA; dI_G/dt = 100 mA/µs; T2- G-	-	50	A/µs
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C
I_{TSM}	non-repetitive peak on-state current	full sine wave; t_p = 16.7 ms; $T_{j(init)}$ = 25 °C	-	8.5	A
		full sine wave; t_p = 20 ms; $T_{j(init)}$ = 25 °C; see Figure 2 and 3	-	8	A
I^2t	I^2t for fusing	t_p = 10 ms; sine-wave pulse	-	0.32	A^2s
$P_{G(AV)}$	average gate power		-	0.1	W



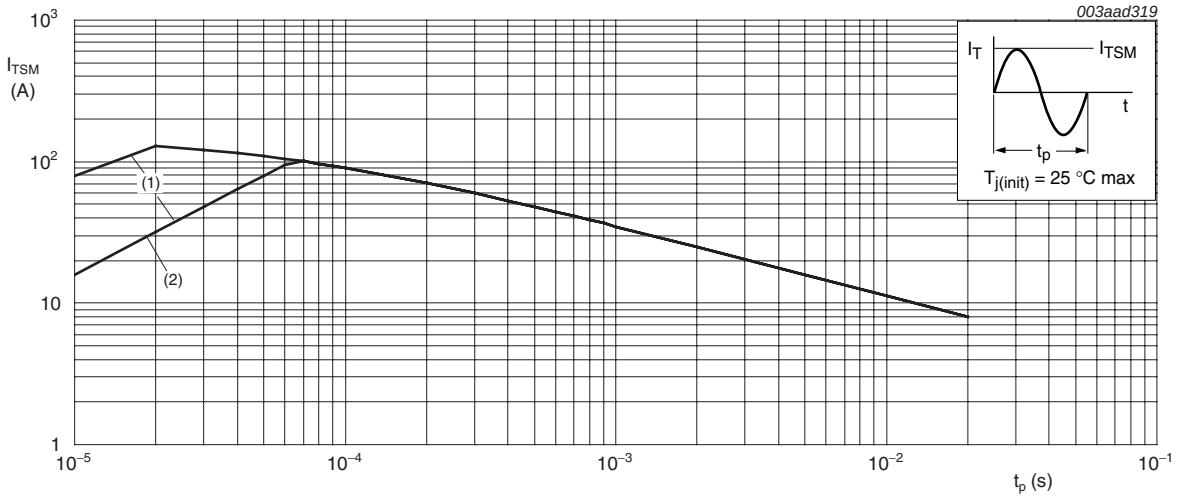
α = conduction angle

Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms; (1) is dI_T/dt limit; (2) is T2 – G + quadrant limit

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

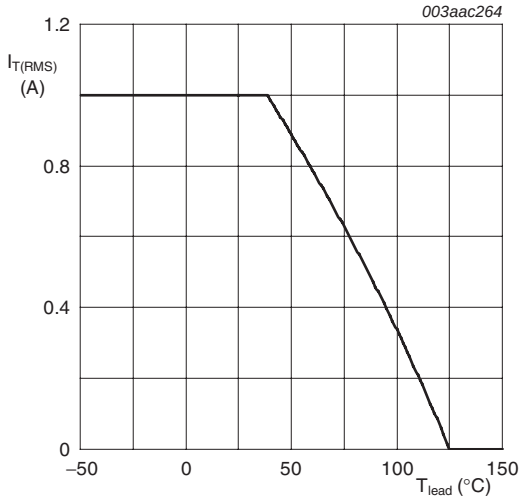


Fig 4. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	150	-	K/W
$R_{th(j-lead)}$	thermal resistance from junction to lead	Full cycle; see Figure 5	-	-	60	K/W

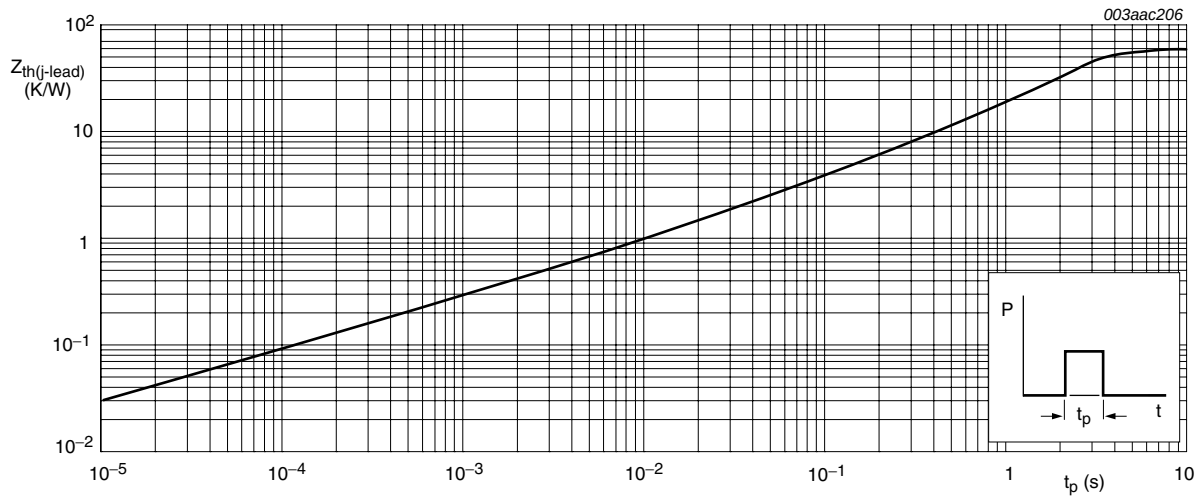
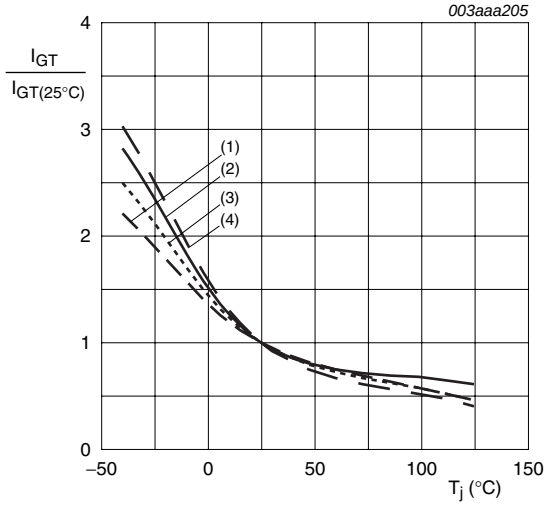


Fig 5. Transient thermal impedance from junction to lead as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; T_j = 25 °C; T2+ G-; see Figure 6	-	-	10	mA
		V_D = 12 V; T_j = 25 °C; T2- G-	-	-	10	mA
		V_D = 12 V; T_j = 25 °C; T2+ G+	-	-	10	mA
		V_D = 12 V; T_j = 25 °C; T2- G+	-	-	10	mA
I_L	latching current	V_D = 12 V; T_j = 25 °C; I_G = 0.1 A; T2+ G-; see Figure 7	-	-	25	mA
		V_D = 12 V; T_j = 25 °C; I_G = 0.1 A; T2+ G+	-	-	15	mA
		V_D = 12 V; T_j = 25 °C; I_G = 0.1 A; T2- G+	-	-	15	mA
		V_D = 12 V; T_j = 25 °C; I_G = 0.1 A; T2- G-	-	-	15	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; see Figure 10	-	-	10	mA
V_T	on-state voltage	I_T = 1 A; see Figure 8	-	1.3	1.6	V
V_{GT}	gate trigger voltage	I_T = 0.1 A; V_D = 12 V; T_j = 25 °C; see Figure 9	-	-	1.3	V
		I_T = 0.1 A; V_D = 600 V; T_j = 125 °C	0.2	-	-	V
I_D	off-state current	V_D = 600 V; T_j = 125 °C	-	-	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 110 °C; gate open circuit; see Figure 11	50	-	-	V/µs
dV_{com}/dt	rate of rise of commutating voltage	V_D = 400 V; T_j = 110 °C; dI_{com}/dt = 0.44 A/ms; gate open circuit	2	-	-	V/µs



(1) is T2+G+ quadrant; (2) is T2+G − quadrant;
(3) is T2 − G − quadrant; (4) is T2 − G+ quadrant

Fig 6. Normalized gate trigger current as a function of junction temperature

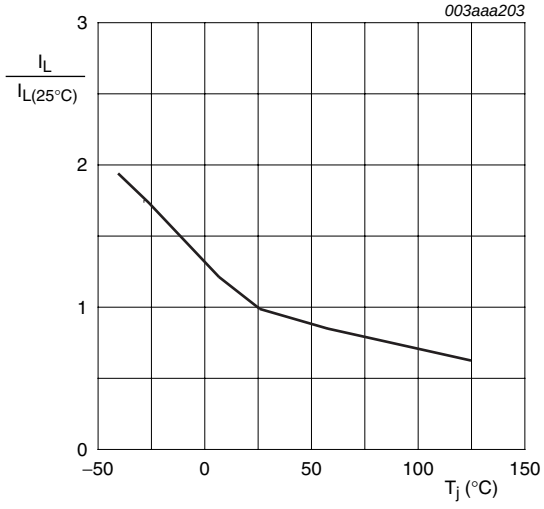
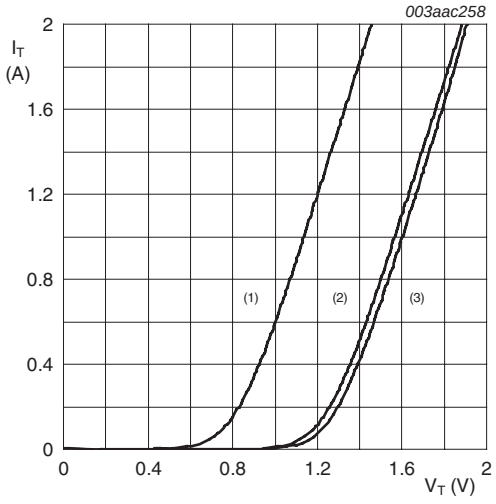


Fig 7. Normalized latching current as a function of junction temperature



$V_0 = 1.254$ V; $R_s = 0.31\ \Omega$
(1) $T_j = 125$ °C; typical values
(2) $T_j = 125$ °C; maximum values
(3) $T_j = 25$ °C; maximum values

Fig 8. On-state current as a function of on-state voltage

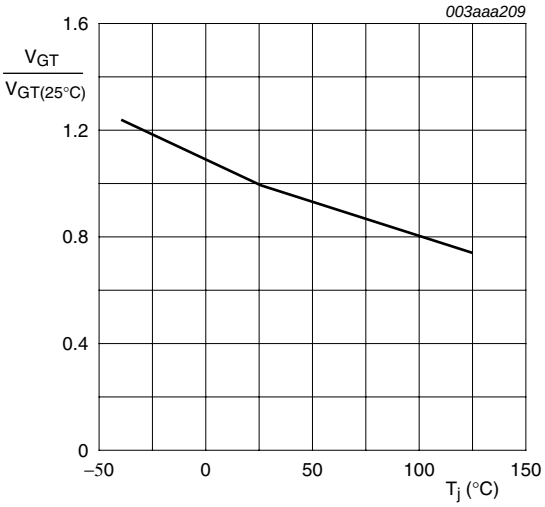


Fig 9. Normalized gate trigger voltage as a function of junction temperature

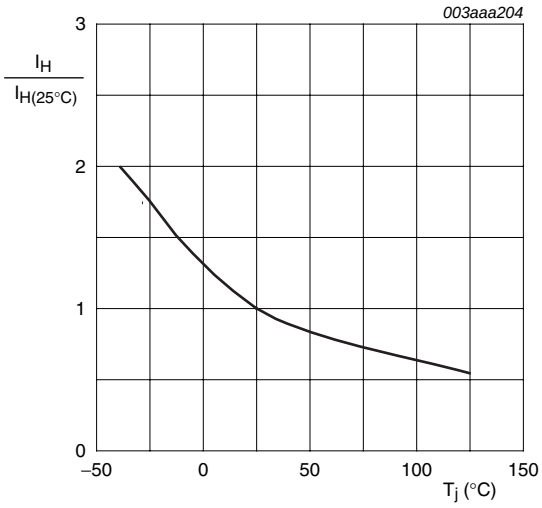
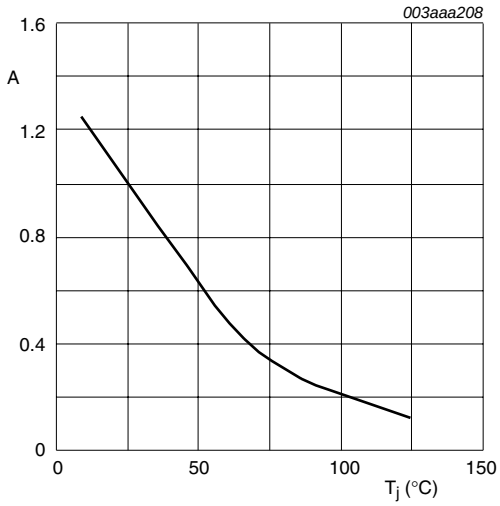


Fig 10. Normalized holding current as a function of junction temperature

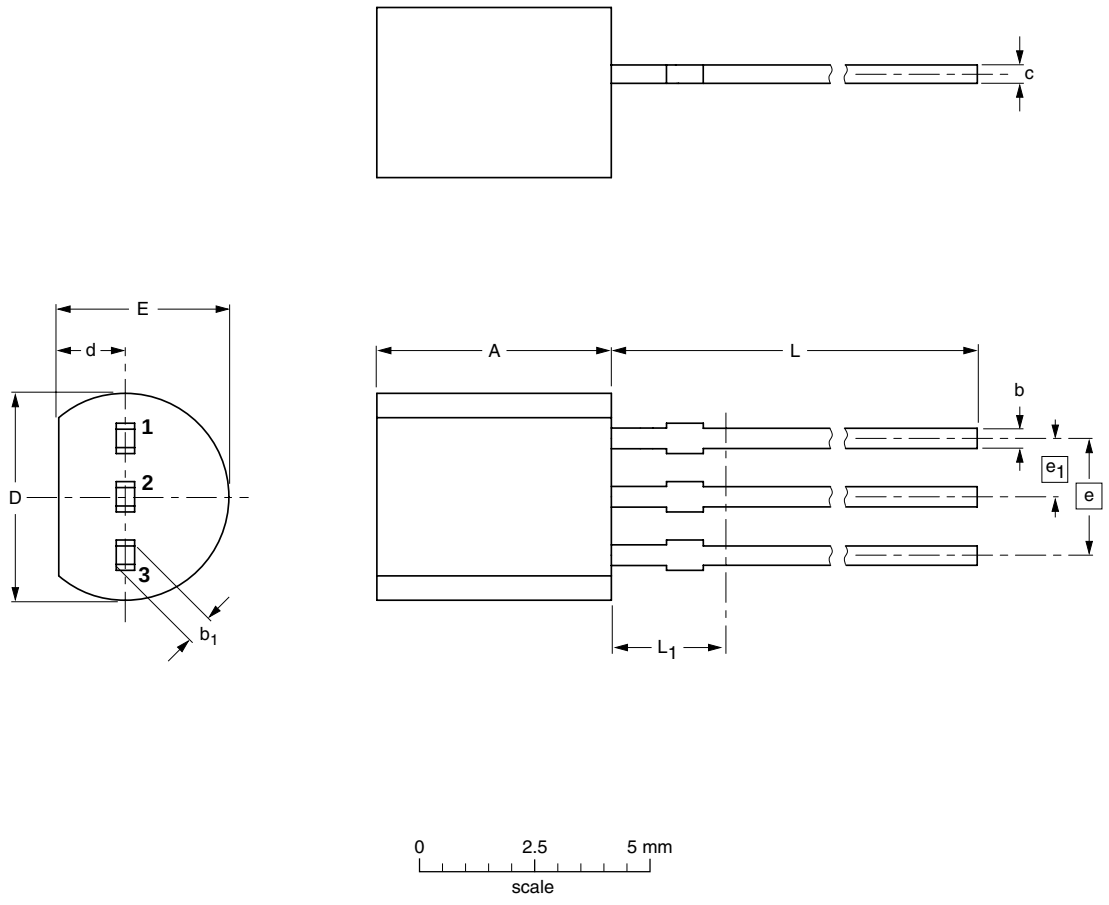


$$A = \frac{dV_D/dt}{dV_{D(25°C)}/dt}$$

Fig 11. Normalized critical rate of rise of off-state voltage as a function of junction temperature;typical values

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig 12. Package outline SOT54 (TO-92)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
Z0109MA_3	20090804	Product data sheet	-	Z0103_07_09_SERIES-02
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number Z0109MA separated from data sheet Z0103_07_09_SERIES-02.			
Z0103_07_09_SERIES-02 (9397 750 10102)	20020912	Product data	-	Z0103_07_09_SERIES-01
Z0103_07_09_SERIES-01 (9397 750 09419)	20020411	Product data	-	-

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9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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